SEMICONDUCTOR MEMORY, AND ITS CONTROL METHOD

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Abstract of **JP2002074957**

PROBLEM TO BE SOLVED: To provide a semiconductor memory in which the current consumption can be reduced sufficiently and the operation speed can be increased sufficiently without increasing the circuit scale, even if increasing the capacity and increasing the operation speed are performed with a low power source voltage. SOLUTION: The short circuit part of a pre-charge circuit Pre3 is constituted of series connection of transistors TN1A, TN1B, transistors TN2A and TN2B are connected in series between a connection point of both transistors and pre-charge voltage VPR and made a potential holding circuit, and the transistors TN1A and TN2A, TN1B and TN2B are controlled respectively by pre-charge signals BRS0, BRS1. Either of the pre-charge signals BRS0, BRS1 is pre-set before one cycle, at the same time the other is set, short circuit operation of a pair of bit line/BL-BL is started, at the time of finish of short circuit operation, a preset side is reset and short circuit operation is finished.